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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,568	11/01/2001	Craig Nemecek	CYPR-CD01214M	5636

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,568	NEMECEK ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in Office Action dated 19 May 2005. Applicants' response dated 18 August 2005 has amended claims 1, 7, 8, 10, 12, 13, 16, 18, and 20. Claims 1-20 have been submitted for reconsideration. Claims 1-20 have been rejected.

Priority

1. This Application contains a claim for the benefit of priority to U.S. Provisional Application No. 60/243,708 filed 26 October 2000. The provisional application has been reviewed and priority is denied, because the provisional application does not appear to enable the claimed invention as required under 35 U.S.C. Section 112, first paragraph. See 35 U.S.C. § 119(e)(1).

For example, the provisional application contains a set of 'powerpoint-style' drawings and datasheets describing desired features for a microcontroller or a 'system-on-chip,' but this material does not appear to contain either the text description or the drawings found in the Application. In particular, no part of the provisional application appears to disclose the method steps shown in the Application at Fig. 7.

Amendments to the Specification

The Examiner thanks Applicants for amending the specification to correct a typographical error with respect to the standard four wire Category Five patch cable. The Examiner has found no new matter in this amendment.

Claim Rejections - 35 USC § 112

The Examiner thanks Applicants for amending the claims in response to the previous rejections under 35 U.S.C. § 112. Those rejections have been withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 5,663,900 to Bhandari et al. (Bhandari) in view of US Patent No. 6,161,199 to Szeto et al. (Szeto).

Regarding claim 1, Bhandari teaches:

An in-circuit emulation system (Figs. 1, 2A, 2B; column 2, lines 31-39, especially "*to provide a simulation environment with computer models to verify the functions of a prototype integrated circuit[s] on a target system*"),

a pod carrying an emulation microcontroller (Fig. 1, references 42, 39; column 2, lines 43-45, "The pod 42 has a male plug-in socket adapter 39 where the adapter 39 connects to the female socket 48 on the target board 46"; column 3, lines 56-60, *external system 46 may be an emulator*),

a base station having a virtual microcontroller that operates in lock-step synchronization with the emulation microcontroller during emulation operations (Fig. 1, reference 10; column 3, line 61 – column 4, line 17, *external system 46 may be implemented on a processor synchronized with primary simulator 16*), and

an interface connecting the pod to the base station (Fig. 1, reference 38) having a clock signal line, a pair of data signal lines, a reset line, and a power line (column 4, lines 3-9, *interface tool enables simulator to interact with various external*

systems; and column 4, lines 10-17, *second simulation tool may be synchronized with primary simulator*, clearly implying a clock signal; column 5, lines 7-15, *interface circuit provides control signals according to instructions and operations from simulator 16 to force, reset, set-up, and initialize pre-determined logic states, etc.*; and column 4, lines 52-62).

Bhandari does not teach a combined microcontroller programmer.

Szeto teaches a non-intrusive in-system debugging apparatus and method that uses an in-system programming mode to program a device such as a microcontroller (column 3, lines 22-33; column 3, lines 42-58). Szeto specifically teaches programming a microcontroller (Figs. 6-7; column 4, lines 1-28).

As Bhandari is a design and verification system, therefore concerned with the ultimate production of the device under design, the advantages of including an in-system programming socket as taught by Szeto would be have been obvious to a person of ordinary skill in the art at the time of Applicants' invention. This combination would join the advantages of the prior art and facilitate both the design and creation of a prototype device. It would have been obvious to implement the programming socket on the pod because the pod is already the existing interface to the emulation microcontroller; any other arrangement would require addition of a redundant interface. In forming this combination, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to take necessary steps to prevent the emulation microcontroller from interfering with the programming socket. Failure to do so would yield an inoperable or unacceptable device.

In response, Applicants argue primarily that:

> [T]he cited combination does not disclose or suggest an interface connecting the pod to the base station, the interface having a reset line connected to transmit a reset signal to the emulation microcontroller without transmitting the reset signal to the socket.
> [...]
> The combined references do not teach, disclose, or suggest the use of a reset signal being transmitted via a reset signal line to one microcontroller but not another microcontroller mounted in the same pod.

The Examiner respectfully traverses this rejection as follows.

As cited above, Bhandari discloses an interface connecting the pod to the base station (Fig. 1, reference 38). As cited above, Bhandari discloses that the interface comprises a reset line and transmitting a reset signal [(column 5, lines 7-15) *interface circuit provides control signals according to instructions and operations from simulator 16 to force, reset, set-up, and initialize pre-determined logic states, etc.*].

As admitted above, Bhandari does not teach a combined microcontroller programmer.

As cited above, Szeto teaches an in-system programming mode to program a device such as a microcontroller (column 3, lines 22-33; column 3, lines 42-58).

The combination formed in the rejection would be within the ability of a person of ordinary skill in the art of in-circuit emulation and programming. The level of skill in this art is particularly high, combining and requiring knowledge of electrical engineering, computer science, computer engineering, system engineering, and other disciplines. Applicants' argument that the combination does not teach transmitting a reset signal to the emulator without transmitting the reset signal to a programming socket is unpersuasive because a person of ordinary skill in the art of in-circuit emulation and programming, when forming the combination used in the rejection, would implement solutions to several trivial problems such as transmitting reset signals as required. Supposing that a system requirement was to reset the programmed

device without resetting the emulator, it would likewise be obvious to a person of ordinary skill in the art to build a system that facilitates that need. These problems and solutions are well within the bounds of what would be known in the art to a person of ordinary skill in electrical engineering, systems engineering, or in-circuit emulation. Therefore, the rejection stands as adequately suggesting to a person of ordinary skill in the art the combined in-circuit emulation system and programmer as claimed in the invention.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 2, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to send programming instructions (the data elements pertaining to the task of programming) to the microcontroller being programmed using the existing data lines taught by Bhandari. It would have been obvious to not use the existing clock line because doing so would drive the emulation microcontroller, a clearly undesirable result. Official notice is communications between electronic devices using a data signal and a clock signal is well known in the art.

Regarding claim 3, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use data lines, as taught by Bhandari, for communicating data.

Regarding claim 4, the combination formed in the rejection of claim 1 includes an interface for communicating with the emulation microcontroller (Fig. 1, connection between references 5, 38, 42, and 39) that is also the interface for programming the microcontroller during programming operations (wherein the programming socket is located on the pod, utilizing the existing connection in Fig. 1, between references 5, 38, and 42).

Regarding claim 5, the combination formed in the rejection of claim 1 would have required connecting the data lines to the terminals of the socket corresponding to programming inputs for the microcontroller residing in the socket, else the device would be inoperable.

Regarding claim 6, official notice is taken that a category five cable is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use a well-known type of cable when connecting the components of the system. Where four twisted pairs of wires are suitable, it would be obvious to use a category five cable, as this type of cable is ubiquitous and economical.

Regarding claims 7, 8, and 10, Bhandari teaches:

An in-circuit emulation system (Figs. 1, 2A, 2B; column 2, lines 31-39, especially "*to provide a simulation environment with computer models to verify the functions of a prototype integrated circuit[s] on a target system*"),

a device under test (column 3, lines 6-20, *simulator verification or testing facility for simulating or emulating a functional specification of a particular prototype definition*),

an interface connecting the pod to a base station (Fig. 1, reference 38) having a clock signal line, a pair of data signal lines, a reset line, and a power line (column 4, lines 3-9, *interface tool enables simulator to interact with various external systems*; and column 4, lines 10-17, *second simulation tool may be synchronized with primary simulator*, clearly implying a clock signal; column 5, lines 7-15, *interface circuit provides control signals according to instructions and operations from simulator 16 to force, reset, set-up, and initialize pre-determined logic states, etc.*; and column 4, lines 52-62).

Bhandari does not teach a combined microcontroller programmer.

Szeto teaches a non-intrusive in-system debugging apparatus and method that uses an in-system programming mode to program a device such as a microcontroller (column 3, lines 22-33; column 3, lines 42-58). Szeto specifically teaches programming a microcontroller (Figs. 6-7; column 4, lines 1-28).

As Bhandari is a design and verification system, therefore concerned with the ultimate production of the device under design, the advantages of including an in-system programming socket as taught by Szeto would be have been obvious to a person of ordinary skill in the art at the time of Applicants' invention. This combination would join the advantages of the prior art and facilitate the design, testing, and creation of a prototype device. It would have been obvious to implement the programming socket on the pod because the pod is already the existing

interface to the emulation microcontroller; any other arrangement would require addition of a redundant interface. In forming this combination, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to take necessary steps to prevent the emulation microcontroller from interfering with the programming socket. Failure to do so would yield an inoperable or unacceptable device.

In response, Applicants argue primarily that:

> The cited combination does not disclose or suggest the use of the data lines of the interface to carry programming instructions to both the device to be programmed and to carry communications with the device under test during emulation operations.

The Examiner respectfully traverses this argument as follows:

Bhandari discloses that *"Cables 41 and 43 provide user-configured signal paths of electrical lines from particular signal pins in sockets or the socket 48 in external system 44, 46 to the target board 38, and thus effectively to particular signal pins specified in the simulated prototype definition"* (column 4, lines 58-62). Further, Bhandari discloses that *"interface circuit 40 includes signal switching circuits or a local processor and memory in board 38 for defining and providing uni- and bi-directional signal paths to couple electrically socket pins in external system 44, 46 to corresponding, representative socket pins in the simulated prototype definition, according to specified interconnection parameters provided to CAE tool 14 by a design engineer"* (column 4, line 63 – column 5, line 2). Therefore, the combination of references at least suggests the use of data lines in the interface to carry communications with the device under test during emulation operations.

Szeto discloses that the in-system programming system, depicted in Fig. 19, includes "connector 1908".

Further, as in the combination formed in the rejection of claim 1, a person of ordinary skill in the art would be confronted with several details of implementation that would be within the capability of and obvious to a person of ordinary skill in the art. One detail of implementation would be the means of communication when programming the microcontroller to carry out the concepts taught by Szeto. In light of the explicit disclosure of an interface connected to the device under test, it would have been obvious to a person of ordinary skill in the art to use that same interface for conducting communication during programming. That is, it would have been obvious, in light of the combined teachings of Bhandari in view of Szeto, to use the data lines of the interface to carry programming instructions to both the device to be programmed and to carry communications with the device under test during emulation operations.

Applicants' arguments have been fully considered but have been found unpersuasive.

Regarding claim 9, official notice is taken that a category five cable is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use a well-known type of cable when connecting the components of the system. Where four twisted pairs of wires are suitable, it would be obvious to use a category five cable, as this type of cable is ubiquitous and economical.

Regarding claim 12, Bhandari teaches several types of devices that may be designed using the disclosed system (column 2, line 64 – column 3, line 5). It would have been obvious to

a person of ordinary skill in the art at the time of Applicants' invention that Bhandari's teachings are clearly applicable to designing a microcontroller.

Claims 13 and 14 recite the method performed by the combination formed in the rejection of claim 1 and are therefore rejected for the same reasons given for claim 1.

In response, Applicants provide arguments that refer to the rationale presented regarding claims 1 and 7, both of which have been addressed above.

Regarding claims 15-16, official notice is taken that write protection using a key code is well known in the art of microcontroller programming. Therefore it would have been obvious to a person of ordinary skill in the art to accommodate transmitting a write enable key to a microcontroller in order to program it.

Regarding claim 17, the combination formed in the rejection of claim 13 includes an interface for communicating with the emulation microcontroller (Fig. 1, connection between references 5, 38, 42, and 39) that is also the interface for programming the microcontroller during programming operations (wherein the programming socket is located on the pod, utilizing the existing connection in Fig. 1, between references 5, 38, and 42).

Regarding claim 18, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to send programming code (the data elements pertaining to the task of programming) using the existing data lines taught by Bhandari. It would have been obvious to not use the existing clock line because doing so would drive the emulation microcontroller, a clearly undesirable result. Official notice is communications between electronic devices using a data signal and a clock signal is well known in the art.

Regarding claim 19, the combination formed in the rejection of claim 13 includes an interface for communicating with the emulation microcontroller (Fig. 1, connection between references 5, 38, 42, and 39) that is also the interface for programming the microcontroller during programming operations (wherein the programming socket is located on the pod, utilizing the existing connection in Fig. 1, between references 5, 38, and 42).

Regarding claim 20, official notice is taken that a category five cable is well known in the art. It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use a well-known type of cable when connecting the components of the system. Where four twisted pairs of wires are suitable, it would be obvious to use a category five cable, as this type of cable is ubiquitous and economical.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892. In particular, US Patent No. 5,371,878 to Coker teaches a debugging and emulation system

for an embedded computer system (ECS) wherein a "shadow system" transfers memory contents from the ECS, thereby executing the same instructions as the ECS in lockstep (abstract; column 2, line 56 – column 3, line 12; etc.) Coker's apparatus is relevant as expressly teaching several major components of the claimed invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Paul L. Rodriguez 10/21/05
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